WHAT IS CLAIMED IS:

1. A method of detecting bit transitions in a serial data stream, the method comprising:

demultiplexing a first bit from the serial data stream;

demultiplexing a second bit from the serial data stream, the second bit adjacent to the first bit;

receiving a recovered clock signal, the recovered clock signal generated at least in part based on the serial data stream;

in response to the recovered clock signal, initiating pattern detection of a pattern defined by the first bit and the second bit;

generating a first output in response to detecting a first pattern defined by the first bit and the second bit;

generating a second output in response to detecting a second pattern defined by the first bit and the second bit;

generating a third output in response to detecting a third pattern defined by the first bit and the second bit; and

generating a fourth output in response to a detecting first pattern defined by the first bit and the second bit.

2. The method as defined in Claim 1, wherein the acts of detecting the first pattern, the second pattern, the third pattern, and the fourth pattern are performed with substantially matched delays.

3. The method as defined in Claim 1, wherein the first output is used to select a multiplicand for a multipliercorresponding to a multiplicand value of zero.

4. The method as defined in Claim 1, wherein the second output is used to select a multiplicand for a multipliercorresponding to a multiplicand value of zero.

5. The method as defined in Claim 1, wherein the third output is used to select a multiplicand for a multipliercorresponding to a multiplicand value of minus one.

6. The method as defined in Claim 1, wherein the fourth output is used to select a multiplicand for a multipliercorresponding to a multiplicand value of one.

7. A data transition identifier circuit used to identify data transitions in a network bitstream, the data transition identifier circuit comprising:

a first differential input coupled to a first clock signal;

a second differential input coupled to a second clock signal;

a first true data input;

a first inverse data input;

a second true data input;

a second inverse data input;

a first constant current sink;

a second constant current sink;

a first pattern indicator output;

a second pattern indicator output;

a first transistor having a first base, a first emitter and a first collector, the first base coupled to the first differential input and the first emitter coupled to the first constant current sink;

a second transistor having a second base, a second emitter and a second collector, the second base coupled to the first differential input and the second emitter coupled to the second constant current sink;

a third transistor having a third base, a third emitter and a third collector, the third base coupled to the second differential input and the third emitter coupled to the first constant current sink;

a fifth transistor having a fifth base, a fifth emitter and a fifth collector, the fifth base coupled to the first true data input, the fifth collector coupled to the second pattern indicator output and the third collector, and the fifth emitter coupled to the first collector;

a sixth transistor having a sixth base, a sixth emitter and a sixth collector, the sixth base coupled to the first inverse data input, the sixth collector coupled to the fourth collector and the first pattern indicator output, and the sixth emitter coupled to the fifth emitter and the first collector;

a seventh transistor having a seventh base, a seventh emitter and a seventh collector, the seventh base coupled to the second true data input, the

seventh collector coupled to the sixth collector, and the seventh emitter coupled to the second collector; and

a eighth transistor having an eighth base, an eighth emitter and an eighth collector, the eighth base coupled to the second inverse data input, the eighth collector coupled to the fifth collector, and the eighth emitter coupled to the second collector.

8. The data transition identifier circuit as defined in Claim 7, wherein a delay between the inverted first data input and the first pattern indicator output is substantially matched with a delay between the second true data input and the first pattern indicator output.

9. The data transition identifier circuit as defined in Claim 7, wherein a delay between the first true data input and the second pattern indicator output is substantially matched with a delay between the second inverted data input and the second pattern indicator output.

10. The data transition identifier circuit as defined in Claim 7, wherein a load on the first clock phase input is substantially the same as a load on the second phase input.

11. The data transition identifier circuit as defined in Claim 7, wherein a delay between the first true data input and the first pattern indicator output is substantially the same as a delay between the first inverted data input and the second pattern indicator output.

12. A data transition detection circuit used to detect transitions in a serial bitstream, the data transition detection circuit comprising:

a first data input configured to receive a first serial bitstream data bit;

a second data input configured to receive a second serial bitstream bit, the second serial bitstream bit adjacent to the first serial bitstream data bit, wherein the second input has substantially the same loading as the first data input;

a timing input, configured to receive a timing signal used to initiate the detection of a data transition;

a first output configured to provide an indication that the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of zero, wherein a first delay from the first data input to the first output is substantially the same as a second delay from the second data input to the first output;

a second output configured to provide an indication that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of one, wherein a second delay from the first data input to the second output is substantially the same as a third delay from the second data input to the second output;

a third output configured to provide an indication that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of zero; and

a fourth output configured to provide an indication that the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of one.

13. The data transition detection circuit as defined in Claim 12, wherein the data transition detection circuit is fabricated from silicon-germanium.

14. The data transition detection circuit as defined in Claim 12, wherein the first data input is a differential input.

15. The data transition detection circuit as defined in Claim 12, wherein the timing input is a differential input.

16. The data transition detection circuit as defined in Claim 12, wherein the timing input is used to accept a first clock phase of a clock recovered from the serial bitstream.

17. The data transition detection circuit as defined in Claim 12, wherein the first output is configured to generate a multiplicand having a value of zero.

18. The data transition detection circuit as defined in Claim 12, wherein the second output is configured to generate a multiplicand having a value of zero.

19. The data transition detection circuit as defined in Claim 12, wherein the third output is configured to generate a multiplicand having a value of negative one.

20. The data transition detection circuit as defined in Claim 12, wherein in the fourth output is configured to generate a multiplicand having a value of one.